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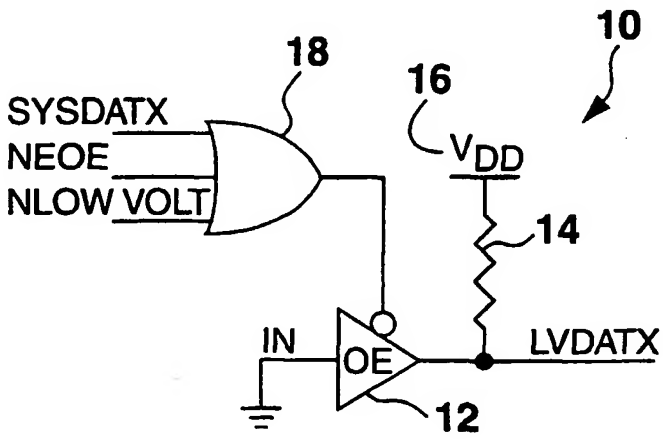
(54) Title: A VOLTAGE TRANSLATOR CIRCUIT WHICH ALLOWS FOR VARIABLE LOW VOLTAGE SIGNAL TRANSLATION



VOLTAGE TRANSLATOR CIRCUIT

(57) Abstract: A variable low voltage signal translator uses a driver (12) for outputting a low voltage signal translation. A control circuit (18) is coupled to the driver (12) for enabling and disabling the driver (12) wherein the control circuit (18) has an input coupled to the signal to be translated. One terminal of the pull-up resistor (14) is coupled to an output of the driver (12). A second terminal of the pull-up resistor (14) is coupled to a voltage supply (16) which provides the low voltage level of the variable low voltage signal translator.

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A VOLTAGE TRANSLATOR CIRCUIT WHICH ALLOWS FOR VARIABLE LOW VOLTAGE SIGNAL TRANSLATION

BACKGROUND OF THE INVENTION

Field of the Invention:

This invention relates generally to a voltage translator circuit and, more specifically, to a voltage translator circuit which uses a tri-state buffer as an open collector driver to achieve high speed variable low voltage signal translation.

Description of the Prior Art:

Presently, low voltage signal translation of a data bus uses a standard buffer device. The buffer is used to translate the data bits on the data bus from a high voltage of approximately 5 volts to a low voltage of approximately 3.3 volts. While present voltage translator circuits do work, the voltage on the low voltage side of the translator is always fixed, or at best, voltage limited.

Therefore, a need existed to provide an improved voltage translator circuit. The improved voltage translator circuit must allow for a variable voltage on the low voltage side of the improved voltage translator circuit. The improved voltage translator circuit must further allow for lower voltage levels to be achieved on the low voltage side of the voltage translator circuit than is currently available with standard buffer devices. The improved voltage translator circuit must also operate at a speed comparable to present circuits.

SUMMARY OF THE INVENTION

In accordance with one embodiment of the present invention, it is an object of this invention to provide an improved voltage translator circuit.

It is another object of the present invention to provide an improved voltage translator circuit that allows for a variable voltage on the low voltage side of the improved voltage translator circuit.

It is still another object of the present invention to provide an improved voltage translator circuit that allows for lower voltage levels to be achieved on the low voltage side of the voltage translator circuit.

It is yet another object of the present invention to provide an improved voltage translator circuit that maintains comparable speed to present voltage limited or fixed voltage circuits.

BRIEF DESCRIPTION OF THE PREFERRED EMBODIMENTS

In accordance with one embodiment of the present invention, a variable low voltage signal translator is disclosed. The variable low voltage signal translator has a driver circuit. A control circuit is coupled to the driver circuit and is used for enabling and disabling the driver. The control circuit has at least one input coupled to a signal that the signal translator is to translate. A resistor has one terminal coupled to an output of

the driver circuit and a second terminal coupled to a voltage supply. The voltage supply is used to supply the low voltage level of the variable low voltage signal translator.

In accordance with one embodiment of the present invention, a variable low voltage signal translator for a data bus is disclosed. The variable low voltage signal translator for a data bus uses a driver for outputting a low voltage signal translation of data on said data bus. A control circuit is coupled to the driver for enabling and disabling the driver. The control circuit has at least one input which is coupled to the data bus to be translated. A resistor has a first terminal coupled to an output of the driver and a second terminal coupled to a voltage supply. The voltage supply is used to supply the low voltage level of the variable low voltage signal translator.

The foregoing and other objects, features, and advantages of the invention will be apparent from the following, more particular, description of the preferred embodiments of the invention, as illustrated in the accompanying drawing.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a simplified functional block diagram of the voltage translator circuit of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Figure 1, a voltage translator circuit 10 (hereinafter circuit 10) is shown. The circuit 10 is used to provide a variable low voltage translation of a data signal. In the preferred embodiment of the present invention, the circuit 10 is used for low voltage emulation of a system processor address and data busses.

The circuit 10 uses an output driver 12. In the preferred embodiment of the present invention, the output driver 12 is a tri-state output driver which is used as an open collector driver to provide an active low drive capability. The input of the output driver 12 is coupled to ground. The output of the output driver 12 is coupled to a first terminal of a pull-up resistor 14. The second terminal of the pull-up resistor 14 is coupled to a voltage supply V_{DD} 16. The voltage supply V_{DD} 16 provides a voltage equal to the low level voltage conversion that is desired.

The output enable (OE) of the output driver 12 is coupled to a control circuit 18. The control circuit 18 is used to enable and disable the output driver 12. In the embodiment depicted in Figure 1, the control circuit 18 is an OR gate. The control circuit 18 will have one or more inputs which are used to enable and disable the output driver 12. In the embodiment depicted in Figure 1, the control circuit 18 has a first input which is coupled to the data signal which is to be translated. In the preferred embodiment of the present invention, the first input (SYSDATx) of

the control circuit 18 is coupled to a data bit of the bus to be translated. The second input (NEOE) of the control circuit 18 is coupled to an output enable signal line of the data bus. In the preferred embodiment of the present invention, the second input (NEOE) is an active low signal which is used to signal when data may be transferred onto the data bus. The control circuit 18 may further have a third input (NLOW-VOLT). The third input (NLOW_VOLT) is used as a master enable to activate or deactivate the output driver 12. In the preferred embodiment of the present invention, the third input (NLOW-VOLT) is an active low input signal.

OPERATION

The low voltage side high level is accomplished by the pull-up resistor 14 and the voltage supply 16. The output driver 12 will either drive the data bit low during a program memory fetch or remain tri-stated to provide a high level via the pull-up resistor 14.

Since the input of the output driver 12 is grounded, once the output enable (OE) of the output driver 12 is driven low to enable, the output of the output driver 12 will output low if the first input (SYSDATx) is low. Conversely, if the output enable (OE) of the output driver 12 is driven high, the output buffer 12 is tri-stated and the pull-resistor 14 pulls the output of the output driver 12 to the desired translated voltage level (i.e., the voltage level of the voltage supply V_{DD} 16).

In the embodiment shown in Figure 1, the output enable (OE) of the output driver 12 is controlled by three signals. The signal NLOW-VOLT serves as a master enable to activate or deactivate the output driver 12. If NLOW-VOLT is high, the output driver 12 will be disabled. If NLOW-VOLT is low, the combination of the other two signals SYSDATx and NEOE will determine the output of the output buffer 12.

The voltage translator circuit 10 addresses the biggest drawback for many voltage translator circuits, namely a lack of speed. Because of the default state of the output is a high level via the pull-up resistor 14, there is essentially no delay for a data bit that is high since the output is already at this state when NEOE is asserted low, and only a small delay for the output driving low.

While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.

What is Claimed is:

1. A variable low voltage signal translator comprising, in combination:

a driver;

a control circuit coupled to said driver for enabling and disabling said driver wherein said control circuit has an input coupled to a signal said signal translator is to translate;

a resistor coupled to an output of said driver; and

a voltage supply coupled to said resistor.

2. A variable low voltage signal translator in accordance with Claim 1 wherein an input of said driver is grounded.

3. A variable low voltage signal translator in accordance with Claim 1 wherein said driver is a tri-stateable buffer.

4. A variable low voltage signal translator in accordance with Claim 1 wherein said control circuit is a logic gate.

5. A variable low voltage signal translator in accordance with Claim 4 wherein said logic gate is an OR gate having a first input coupled to said signal said signal translator is to translate and a second input coupled to a second signal which enables and disables said driver.

6. A variable low voltage signal translator in accordance with Claim 5 wherein said OR gate has a third input coupled to a signal which indicates when data is to be driven on said signal said signal translator is to translate.

7. A variable low voltage signal translator in accordance with Claim 1 wherein said voltage supply supplies a low voltage level of said variable low voltage signal translator.

8. A variable low voltage signal translator for a data bus comprising, in combination:

a driver for outputting a low voltage signal translation of data on said data bus;

a control circuit coupled to said driver for enabling and disabling said driver wherein said control circuit has an input coupled to said data bus;

a resistor coupled to an output of said driver; and

a voltage supply coupled to said resistor.

9. A variable low voltage signal translator in accordance with Claim 8 wherein an input of said driver is grounded.

10. A variable low voltage signal translator in accordance with Claim 8 wherein said driver is a tri-stateable buffer.

11. A variable low voltage signal translator in accordance with Claim 8 wherein said control circuit is a logic gate.

12. A variable low voltage signal translator in accordance with Claim 11 wherein said logic gate is an OR gate having a first input coupled to said data bus, a second input coupled to a processor signal which indicates when said data is to be driven on said data bus, and a second input coupled to a third signal which enables and disables said driver.

13. A variable low voltage signal translator in accordance with Claim 8 wherein said voltage supply supplies a low voltage level of said variable low voltage signal translator.

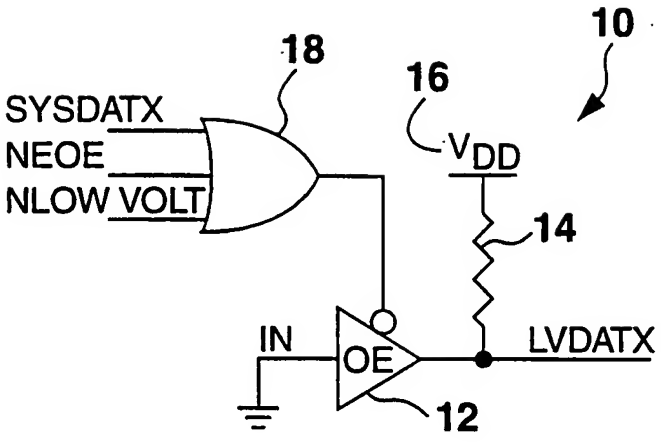
14. A variable low voltage signal translator for a data bus comprising, in combination:

a driver for outputting a low voltage signal translation of said data bus wherein an input of said driver is grounded wherein said driver is a tri-stateable buffer;

a control circuit coupled to said driver for enabling and disabling said driver wherein said control circuit has an input coupled to said data bus wherein said logic gate is an OR gate having a first input coupled to said data bus, a second input coupled to a processor signal which indicates when data is to be driven on said data bus, and a second input coupled to a third signal which enables and disables said driver;

a resistor coupled to an output of said driver; and

a voltage supply coupled to said resistor wherein said voltage supply supplies a low voltage level of said variable low voltage signal translator.



VOLTAGE TRANSLATOR CIRCUIT

Fig. 1

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 99/24569

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03K19/0175

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PACKER L: "OVERVOLTAGE-TOLERANT QUAD BUFFER USED AS VOLTAGE LEVEL SHIFTER" ELECTRONIC DESIGN,US,PENTON PUBLISHING, CLEVELAND, OH, vol. 46, no. 4, 23 February 1998 (1998-02-23), page 128,130 XP000773486 ISSN: 0013-4872	1-3, 7-10,13
Y	the whole document	4,11
Y	"5 VOLT SIGNAL LEVELS FROM 3 VOLT LOGIC" IBM TECHNICAL DISCLOSURE BULLETIN,US,IBM CORP. NEW YORK, vol. 37, no. 3, 1 March 1994 (1994-03-01), page 575 XP000441588 ISSN: 0018-8689 page 575	4,11

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 January 2000	03/02/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Feuer, F

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INTERNATIONAL SEARCH REPORT

Inter ›nal Application No
PCT/US 99/24569

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 017, no. 069 (E-1318), 10 February 1993 (1993-02-10) & JP 04 273717 A (TOSHIBA CORP), 29 September 1992 (1992-09-29) abstract	1,2,4,8, 9,11
A	"5-BOLT SIGNAL LEVELS FROM 3-VOLT LOGIC" IBM TECHNICAL DISCLOSURE BULLETIN,US,IBM CORP. NEW YORK, vol. 37, no. 3, 1 March 1994 (1994-03-01), pages 389-390, XP000441513 ISSN: 0018-8689 the whole document	1-14

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter ›nal Application No
PCT/US 99/24569

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 04273717 A	29-09-1992	NONE	